VG330 POWER MANAGEMENT

A VADEM White Paper

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Introduction

Today, handheld products are providing flexibility and innovation for doing business with unprecedented freedom and mobility. For example, GTE Telephone Operations has equipped its customer service technicians with PDAs, allowing them to receive dispatch, mapping, and diagnostic information. Using PDAs lets technicians spend more time servicing GTE customers on site, which results in fewer off site hours and a significant dollar savings.

Avis has introduced handheld computers at car rental return points, providing a much higher level of customer support. Speedy car returns attract business travelers and their business dollars.

Handheld systems are typically used for data collection and are not computation intensive. They generally provide wireless communications and high user interaction. Handheld systems are expected to last at least one eight hour shift on a single battery charge. OEM developers strive constantly to extend the battery life of the product through power management.

PDAs, handheld computers, and other portable products will become as indispensable as the cellular telephone in future business use. System power management will play a crucial role in achieving optimum product design for long battery life with low weight. But designing a handheld system with excellent battery life is not just a matter of hooking together a few chips and other components to a rechargeable battery. A comprehensive power management solution involves systems knowledge, IC expertise, and software proficiency at the operating system level and at the application level.

Vadem's VG330 power management solution, discussed in this paper, has the following features:

- Highly integrated hardware and software cooperative power management
- SmartClock activity monitoring
- SmartBattery support
- Advanced Power Management (APM) support
- Advanced battery monitoring
- Single-bus chip architecture
- Hardware Power Management Unit
- Peripheral device power management
- Single-chip solution for reduced power

Executive Summary

Vadem – Vadem's focus is on integrated handheld solutions, including single-chip platforms, BIOS, and firmware. The Vadem VG330 is a highly integrated solution that incorporates an x86 32-MHz compatible CPU with core logic, an LCD controller, keyboard controller, real time clock, PCMCIA controller and Vadem's latest generation Power Management Unit (PMU).

Vadem provides industry standard Advanced Power Management (APM) firmware, which takes full advantage of more than 20 innovative chip features in the VG330, thus reducing the time-to-market for OEMs. BIOS source code is optionally available to system designers wishing to further customize power management in their own environment. System cost is always of concern, and the VG330 with its full complement of 24 general purpose I/O pins can easily integrate SmartBattery management and other peripherals without extensive glue logic. Some systems that might have required a microcontroller for sophisticated battery monitoring can eliminate that chip, further reducing cost.

The VG330 and the VG230, the first generation of single-chip microprocessor platform, have the lowest effective power consumption in their class. Vadem understands application requirements and system implementation techniques, and has developed complete solutions that include both hardware and software.

Cooperative Power Management – Hardware and software cooperative power management is the preferred approach to maximize system power savings. Vadem's power management solution consists of both hardware and software elements, as explained in the following subsections.

Hardware Power Management Support – Hardware power management support especially benefits systems running applications and operating systems that are not power management aware. Hardware power management support on Vadem's single-chip VG330 single chip platform consists of the following:

- SmartClock—see Appendix A
- Power Management Unit (PMU)—see Appendix B
- Advanced Battery Monitoring—see Appendix C
- Unified Memory Architecture

The Power Management Unit provides the following well-defined power states to save power:

- ON
- DOZE
- SLEEP
- SUSPEND
- OFF

The PMU provides hardware power management timers, hardware activity monitors, and I/O trapping interrupts that can monitor peripheral device activity. SmartClock and StopClock features permits flexible CPU clock control during operation. See Appendix A and Appendix B for more details.

Advanced Battery Monitoring safeguards user data, even in systems that do not use a backup battery. Resume Abort and Resume Lockout features may eliminate the need for a microcontroller for this purpose. Low Battery 1 (LB1) and Low Battery 2 (LB2) signals support low battery warning and critical suspend. See Appendix C for more details.

The Unified Memory Architecture eliminates a separate video RAM, provides greater CPU bandwidth for video, and saves power.

Software Power Management Support – Software power management can work together with VG330 hardware to provide the best solution. All software levels can benefit—OS, drivers, and Advanced Power Management (APM) BIOS— resulting in maximum power savings with excellent system response. Vadem offers its APM BIOS and the BIOS Adaptation Kit to support OEM power management customization.

The APM specification was defined by Intel and Microsoft and is supported by most DOS vendors. It describes an interface between the system BIOS and the DOS power management driver to cooperatively manage the system power. APM provides a way for the DOS power management driver to set the power state and query the battery level in the system. The DOS level power management driver can also poll the APM BIOS for power management events such as suspend requests or resume notifications. It can then act on these notifications to inform other device drivers and, when appropriate, command the system to go into the suspend state.

Power/Performance Tradeoffs – Flexible power/performance tradeoffs and configuration with bus power management options reduce power consumed by the system. Peripheral devices can be closely power managed with the highly integrated VG330 design. The VG330's internal LCD controller, serial controller, and PCMCIA controller all support power saving modes.

What is Power Management?

Power management can be defined as the collection of techniques that extend battery life in handheld devices while meeting user performance requirements. Two major requirements are:

1. The device must perform well when operating
2. The device must be maintained on reduced power when idle

Good power management trades off performance for power. System data integrity relies on advanced battery monitoring. Power management hardware must be powerful enough to do the job, yet must work well with system software to complete the solution. All these topics will be addressed in the sections below.

Power Management by Design

IC vendors developing power management solutions understand that there are several design options. The most effective power management starts with a good understanding of the hardware, the operating system, and typical application usage. Power management can be applied at the following levels:

- Product Architecture
- Hardware System
- Operating System
- Application
- Component

Product Architecture Level – The OEM System Designer can design in power savings when the product architecture is first defined. The choice of devices and their data widths and configurations is the first design decision that significantly impacts power and performance. The system designer can next determine the programmable configuration options that will save power in his implementation. The choice of operating system or addition to the operating system of power aware device drivers can also greatly affect power consumption.

Hardware System Level – At the hardware system level, power savings can be realized through integration of a multi-chip solution, which reduces the system component count. Most of the power consumption in ICs occurs with I/O pin drivers. It takes a very small driver with a correspondingly small power consumption to drive a signal internally compared with driving an off-chip peripheral. Integration also permits a closer monitoring of the different components of the system (display, interrupt controller, serial interface, and so on) because signals from the internal peripheral blocks are readily accessible. A single bus architecture, such as that provided with the VG330, means the LCD controller does not require a separate RAM device in the design, so fewer pins are used and less power is consumed.

System performance per milliwatt can be determined. The system can be run at various speeds and system performance measured and plotted. Results can be analyzed and system performance tuned accordingly to minimize power. The flexibility of Vadem power management facilitates this process.

Operating System Level – At the OS level, power savings can be achieved in the device drivers. The operating system should reduce power when idle. System peripherals should be shut down when not in use. Hardware resources should be controlled as tightly as the operating environment permits.

Application Level – Key applications should be modified to eliminate busy waiting whenever possible. A power management aware application optimizes idle loops inside the application software to realize the highest level of power savings.

Component Level – A system's power requirements are determined by the operating power requirements of the components. Overall, lower voltage and lower frequency components require less power. The CPU, then, should be of a static design, operating at 3.3 volts or less. The VG330 is such a CPU and accommodates input clock frequencies from 0 -Mhz to 32-MHz.

CPU power increases as peak performance increases, so the system designer should determine the performance requirements and design in what is needed, not what is desired. Larger CPUs require more power not only due to more pins switching at a greater frequency, but also due to the larger number of gates switching. The 20K gate 8086 compatible cores require less power than the 100K gate 386/486 cores

Power Management Philosophy at Vadem

Vadem's power management philosophy is based upon a hardware and software cooperative approach to achieve maximum power savings. Vadem's power management solution was developed by an architecture team composed of chip hardware and system firmware engineers who understand system requirements, behavior profiles of operating systems, drivers, and end applications. This resulted in the VG230, Vadem's first generation single-chip microprocessor platform, which allowed OEM system designers to reach a wireless communications enabled solution that operates for at least a full 8 hour shift.

Increasing demands in the marketplace and close cooperation with OEM customers focused on high volume, battery operated handhelds led Vadem to significantly enhance the already successful VG230 power management for use with the VG330. The VG330 additionally provides a flexible set of hardware options and operating modes that integrate smoothly with your software to save power.

Typical Power Management Solutions – Traditionally, power management solutions come from the following markets:

- Microcontroller Systems
- PC Laptop

Microcontroller power management solutions typically consist of a few hardware features.

PC Laptop power management solutions rely on System Management Mode (SMM), which is an expensive, chipset-oriented firmware/hardware approach.

Default Hardware Only Power Management – With hardware power management, power management decisions are based on hardware activity only, not software activity. The system firmware provides default power management before the operating system is loaded and software power management control begins. The Power Management Unit of the core logic monitors hardware activity of various subsystems based on the hardware activity shown in Table B-1 on page 16.

Typical hardware-only power management schemes slow the CPU clock when no activity is detected. However, hardware only power management cannot discriminate between an idle program and a program that is compute bound (busy, yet not moving data to the I/O devices).

Software Power Management – Software cooperative power management is the preferred approach, and incorporates both hardware and software activity monitors into the power management solution.

A software activity monitor monitors operating system software activity and provides indirect control of power management by the operating system. Indirect control of power management permits existing driver software to run on the system without modification and provides good power management.

A software activity monitor can detect activity that is indicative of busy waiting—constant polling of keyboard queue status, or of other software interfaces. When busy waiting is detected, the power management driver can slow the system down. The software activity monitor will see no activity if an application is doing a compute-bound task—for example, a spreadsheet recalculation. In this case, the software activity monitor can operate either aggressively by slowing down the system, or conservatively by leaving the system operating at full speed. Hardware only activity monitoring would assume that the system is idle and slow the system down, which impacts user performance.

A software activity monitor is an example of indirect control of power management by the operating system. The operating system does not know directly whether the system is active or idle, but uses decision rules based on activity monitoring to set the CPU speed. Direct control of power management by the operating system is better. Maximum power savings can be achieved by an event-driven operating system that directly determines the CPU speed for various tasks depending on priority. The idle task stops the CPU clock until the next interrupting event.

SmartClock – The handheld market requires a higher level of power management with hardware and operating system software integration. A technique has been identified that operates under software power management control and automatically modulates the hardware CPU clock. The events that cause CPU clock modulation are not the same as the events that impact longer duration timeouts, such as LCD timeout and suspend timeout. This technique is called SmartClock and is detailed in Appendix A.

SmartClock is a technique that exemplifies the cooperative hardware/software approach to power management for providing quick response to changing system conditions.

Relative Response Times – Power management can be realized through efforts at the application level, the BIOS level, and the IC level. Each level operates on different time scales. For example, the response time for power management at the IC level might need to be measured in microseconds, while at the application level, a response time of seconds is usually acceptable. Vadem, with its combination of hardware and BIOS solutions, spans both the microsecond and millisecond range as shown in the table below.

Level	Response Time
Application	seconds
BIOS	milliseconds
Hardware	microseconds

Typical handheld systems require a very fast response to loss of battery power. The power management software must be able to suspend the system in a matter of milliseconds. For example, such a case could occur when the user changes batteries or when the system is dropped and the batteries momentarily bounce away from their contacts and disconnect.

VG330 Hardware Design Options for Power Savings

The VG330 supports power management through dedicated hardware consisting of two main features:

- Power-Optimized Single Bus Architecture
- Power Management Unit.

These are individually described. Advanced Battery Monitoring is a hardware specific topic that benefits battery operated systems and is included in the hardware resource description.

Power-Optimized Single Bus Architecture – The VG330 provides the following bus management and configuration options to help the OEM designer produce a low power design:

- **Scaleable Address Bus**—reduces power by reducing number of signals.
- **Bus Inhibit Mode**—inhibits system bus activity during I/O cycles to internal devices, which reduces signal transitions on the bus and saves power.
- **Bus Latching Mode**—reduces bus address width during accesses to specified devices like ROM and RAM, which reduces signal transitions on the bus and saves power. Upper address pin configuration defines the address width of system ROM and RAM.
- **Data Hold Option**—decides whether the system data bus is driven to zero or last data during idle bus cycles. Data Clamping decides whether the system data bus is driven to zero or tri-stated during processor stop clock HALT bus cycles. These options can be selected to minimize power of the system.
- **Expansion Bus Mode Options**—control whether system clock signal SYSCLK is continuous or only clocked when accessing an external device. This reduces SYSCLK signal transitions on the bus and saves power.

In addition, the following design choices are available to the system designer that will trade off performance for power savings.

- Most applications need the performance of 16-bit wide RAM and ROM data paths. In general, a single 16-bit RAM consumes less power than two of 8-bit RAMs.
- DRAM gives better performance than PSRAM due to page mode.
- Self-refresh RAMs lower suspend power.
- Performance of ROM code can be improved using RAM shadowing.
- Refresh timing can be adjusted for slower refresh RAMs to reduce refresh overhead, which improves performance.

The VG330 supports a Single Bus Architecture. Consequently the video subsection does not need a separate video RAM. The Single Bus Architecture reduces the number of components in the system but, more importantly, reduces the overall power consumption for the system. The video controller is integrated into the system, so video performance is not penalized. The architecture delivers performance equivalent to an external LCD controller residing on the local bus.

Power Management Unit – The VG330's Power Management Unit (PMU) consists of all the hardware required to control power intelligently. The PMU includes control registers, timers, and power supply connections to the various sub-systems such as the LCD controller, System RAM, and so on. Every functional block within the VG330 has been designed to minimize power consumption. For details on the PMU, see Appendix B, "Power Management Unit."

Power Management of Peripheral Devices

LCD Controller – The VG330 LCD controller supports completely transparent power control. Software can access the display buffer and LCD controller registers even after the power to the LCD has been shut down and display refresh has been stopped. This means that no software intervention or monitoring is required—the hardware PMU LCD timer controls the display power. There is no impact on existing software, which can run without any change.

Serial I/O (SIO) – SIO power control is most effective at the device driver level. The SIO Activity Timer can transparently save power with most protocols to stop the SIO baud clock until receive/transmit starts. The SIO buffer and IR LED drivers can be powered down when serial communications are disabled.

PCMCIA Controller – The PCMCIA controller supports power control of the PCMCIA socket. Power may be on or off to the PCMCIA card during suspend. If power is left on, the system may be awakened by the Ring Indicator signal from a modem card.

Inactivity timeouts for memory cards in the PC card slots are typically provided by the DOS PCMCIA device drivers. When a timeout interval expires, the socket is powered off, which means that a startup delay is incurred on the next access to the memory cards.

DOS PCMCIA device drivers typically do not power manage I/O PCMCIA cards because the application accesses some devices directly at the hardware level (for example, modem cards). However, it is recommended that power aware applications or PCMCIA card specific device drivers be developed or acquired that shut down inactive cards due to the large power requirements of typical PCMCIA I/O cards.

PCMCIA ATA cards have power management features that are enabled by the DOS PCMCIA device drivers. These cards are placed into low power modes after inactivity timeouts.

Summary

Vadem VG330 power management provides the best power management for its class. This performance is possible due to the early adoption of a hardware/software cooperative approach, providing in hardware the features and controls required by software to implement power management. Vadem provides the BIOS software with APM support to complement the hardware, enabling the OEM developer to deliver solutions faster to the market.

Many OEM developers will be able to see excellent power management off-the-shelf. For systems where every last bit of power has to be reduced, the Vadem VG330 solution gives the OEM developer the flexibility and features to achieve their power management goals.

Appendix A
SmartClock

Near Idle Events

A substantial portion of event-driven system operation occurs during near idle conditions (for example, keystroke capture). The near-idle events can be handled without compromising system response time merely by operating the CPU at a faster rate for the critical interrupt handling of the event and then falling back to a slower clock for less critical operations. Accumulation of several near-idle events can then be construed as an indication of more demands being placed on the system, and the clock speed can be accelerated and maintained at a higher speed rather than shifting down immediately upon completion of the event.

Activity Indicators

SmartClock uses a separate definition of activity to control the CPU clock on a time scale of microseconds. The SmartClock Activity monitor is used to control the CPU clock and does not interfere with the much longer Sleep or Suspend timeouts.

SmartClock monitors the following indicators of activity:

- Programmable I/O range
- Video buffer writes
- IRQ activity
- Serial port accesses
- PC Card accesses
- Keyboard port accesses
- Programmable chip select accesses

When the above indicators are enabled, they signal the system to return to full speed immediately or as quickly as the OEM requires.

SmartClock activity indicators are used as inputs into the SmartClock level counter. When activity is detected, it immediately causes an increase in the activity level (only if the activity latch is reset) and the activity latch is set. The activity latch is checked and reset every tick of the sample clock and the activity level is decreased if there had been no activity in that time interval. When activity level reaches zero, the CPU clock is slowed or stopped. When activity level reaches maximum, the CPU clock becomes maximum. This mechanism provides a system with hysteresis which can be adjusted to keep CPU clock slow during system idle, yet speed up after detection of significant activity (activity level reaches maximum).

Power Management Intervals

SmartClock manages power over short time intervals (microseconds) while traditional power management manages power over long time intervals (milliseconds to seconds). SmartClock can monitor system activity and control CPU speed with no software overhead and practically no power consumed, therefore it is feasible to manage power over shorter time periods than possible with software approaches, such as System Management Mode(SMM). SmartClock can be configured to run in hardware only or software cooperative modes.

System performance can be tuned more finely when SmartClock is enabled. SmartClock enables the average performance to be adjusted by increasing the fast clocking time interval in response to activity, thereby increasing the ratio of time the CPU is operating fast versus slow.

DOS Solutions

Power management solutions are available now from many DOS suppliers. For example, MS-DOS POWER.EXE device driver uses the APM interface to BIOS to get power management events and then communicates them to power-aware device drivers.

One problem in the DOS environment is that of DOS application idle loops. When the application is running full speed and doing nothing in an idle loop, how can it be detected? If the idle loop is polling keyboard, then POWER.EXE will detect pattern of activity which indicates BUSY WAIT. If the idle loop is polling some other device, then POWER.EXE can be modified to detect this pattern of activity either by way of software or hardware activity status monitoring.

SmartClock was especially designed for operation with DOS power management. The SmartClock timer resolution is in Microseconds while the Doze timer is in Seconds. Hysteresis is used to discriminate between minor and significant activity. The PMU can detect significant activity in short period of time and respond quickly (hardware speeds) to operate at full clock speed, for example screen repaints and scrolling. The system can then DOZE between keystrokes.

SmartClock provides power on demand to applications and drivers. Power management software can reduce the main clock rate to the CPU and LCD devices or set the machine state into DOZE or use HLT to lower power until next interrupt event. SmartClock will reduce CPU clock rate until interrupt goes active, when CPU clock rate goes to full speed and remains full speed until an adjustable inactivity time period.

The problem of identifying when a program is idle and not busy waiting is solved in an event-driven environment like Geoworks or a RTOS. All programs can eliminate busy waits in polling loops by calling the OS WaitForEvent routines where applicable, and include the OS WaitForTime in the program polling loops. The OS level would then actively reduce power while waiting using APM.

Smartclock can be used to transition to fast speed immediately on Smartclock Activity detection, and transition to fast speed after time interval when no Smartclock Activity is detected. The OS Idle task will call APMCPUIdle or can be customized to perform similarly. The VG330 will run slowly after the CPUIdle call, because the CPU Idle call is a good predictor of future idle states. When the system is busy, then system will then automatically return to fast speed.

The SmartClock approach relies on the hardware power management features to monitor activity and run fast during critical I/O operations and interrupts, run slow during any idle loop in the OS, and yet respond to compute bound situations by running fast.

Appendix B
VG330 Power Management Unit

PMU State Machine

The VG330 Power Management Unit state machine controls the system power states and the transitions between them as follows:

- **ON—**The ON state is full speed, full power. When no activity is detected for a timeout period of 0.125 to 14 seconds, the ON state automatically becomes the DOZE state.
- **DOZE**—The DOZE state is transparent power savings. DOZE state provides a power savings state that is completely transparent to the user by modulating the speed and power, which means that the system performs as well as it does in ON mode—software responsiveness, performance, and capabilities are identical to the user. When SmartClock is enabled, the CPU clock speed is modulated by the system load. When no activity is detected for timeout period of 1 to 15 minutes, an NMI will be typically generated to allow the software to control the state transition. The DOZE state can change to either the SLEEP or SUSPEND states.
- **SLEEP**—The SLEEP state is a state with reduced capabilities and power savings. The SLEEP state can be used to shutoff a major subsystem with a long timeout, typically when it is not transparent to system operation, such as a disk drive or LCD backlight. In a system with a backlit LCD where the LCD can be used without the backlight on, the LCD backlight can be timed out by defining the SLEEP state to be system with backlight OFF. When SmartClock is enabled, the CPU clock speed is modulated by the system load. When no activity is detected in the SLEEP state for timeout period of 1 to 15 minutes, an NMI will be generated to allow the software to control the next state transition, which is typically the SUSPEND state.
- **SUSPEND**—The SUSPEND state is the lowest power state. When the system is suspended, it draws the lowest amount of power and only wakes up when signaled by the power on/off switch, RTC alarm, or Ring Indicator. Suspension of a handheld unit typically means stopping the clock to the CPU, saving the state of a limited number of devices, and powering down the external devices. The VG330 and RAMs remain powered in a low power suspend state that saves their contents. The VG330 remains suspended with a typical 10 microamp current draw. A handheld system, unlike a Laptop Computer, does not have a hard disk and needs no SaveToDisk feature.
- **OFF**—In the OFF state, all power is removed from the system except for the Real Time Clock.

Clock Speed Control

The CPU clock speed can be changed to trade off power and performance. The CPU block and memory array consume the most power in the system. Their consumption is roughly proportional to clock speed. The BCG Mode Register (index 1) controls the system clock rate with programmable divisors of 1,2,3, or 4 and dynamically change the maximum clock rate to the CPU and the LCD controller.

The PMU may further divide down the CPU clock, and the LCD controller will further divide down the clock for the LCD. Slowing the input clock to the CPU and LCD blocks reduces power. The LCD T1-T4 Registers (3D4 index C6-C9) determine the LCD dot clock and other timing. When the clock is dynamically controlled with the BCG Mode register, the LCD controller is impacted and the LCD timing needs to be changed simultaneously.

The PMU sets the following CPU speeds:

- Fast Clock
- Slow Clock (divided by 4 or 8)
- Stop Clock

If the SmartClock option is enabled, clocking is automatically modulated by the processing load. The PMU speeds up the clock during NMI and IRQ routines to ensure that realtime data is handled quickly.

Clock Control Register

The Clock Control register provides the following options to tradeoff performance and power savings.

- Stop Clock on Halt reduces power consumption by the bus devices when a HALT cycle is run.
- Stop Clock on Expansion Bus Cycle reduces power consumption of the CPU core during wait states or when waiting for the Ready signal. This reduces somewhat the pipelining during CPU operations.
- Stop Clock on Non-Busmaster Cycles reduces power consumption of the CPU core when waiting for control of system bus to return to CPU. This reduces somewhat the pipelining during CPU operations.

Power Management Activity Monitor

The VG330 activity monitor detects important system operations. It does this by monitoring the following hardware events:

- Interrupts
- System Peripheral I/O Cycles
- Video Memory Write Cycles

The above events are indications that the system is performing tasks that should be executed at full speed. Lack of system activity is usually, but not always, an indication of an idle system. In addition, more detailed peripheral device status can be monitored by I/O trapping if required.

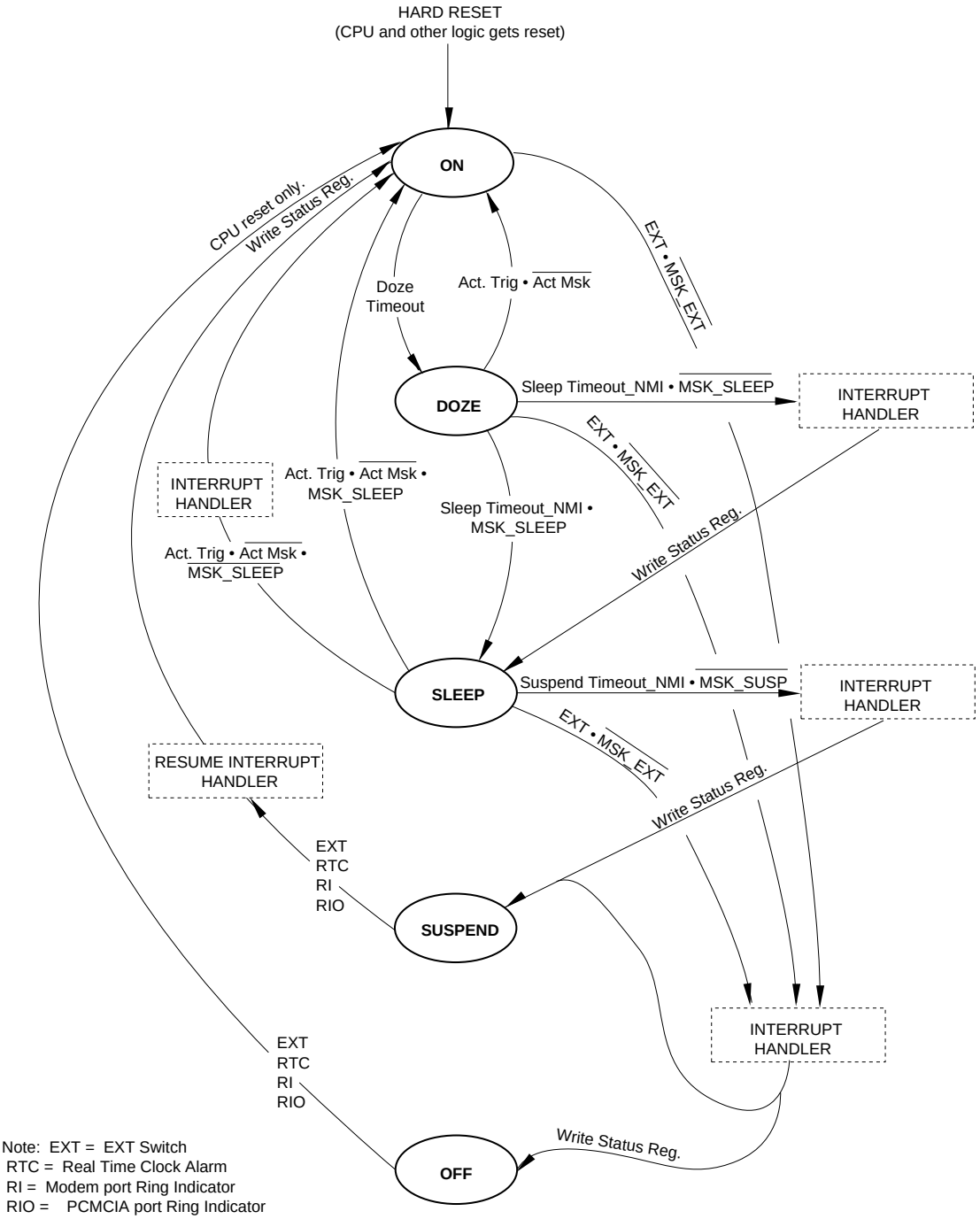
Table B-1 summarizes the activities monitored by the PMU.

Table B-1
PMU Hardware Monitoring

Hardware Monitored	Address
Parallel Printer Port	I/O R/W access to LPT1–LPT3
LPT1	378h–37Fh
LPT2	278h–27Fh
LPT3	3BCh–3BEh
Keyboard Port	I/O Reads to port 60h
Serial I/O	I/O R/W access to COM1 and COM2
COM1	3F8h–3FFh
COM2	2F8h–2FFh
Floppy Disk	I/O R/W access to 3F5h
Hard Disk	I/O R/W access to XT or AT hard disk
XT disk	320h–323h
AT disk	1F0h–1F7h
Video Memory Access	Write access to video memory, typically B8000h - BFFFFh
Programmable I/O	See description of PMU I/O Range register IORNG
PC Card	Reads/writes to PC Card I/O ports or memory

Figure B-1 illustrates the PMU state machine.

Figure B-1
PMU State Diagram



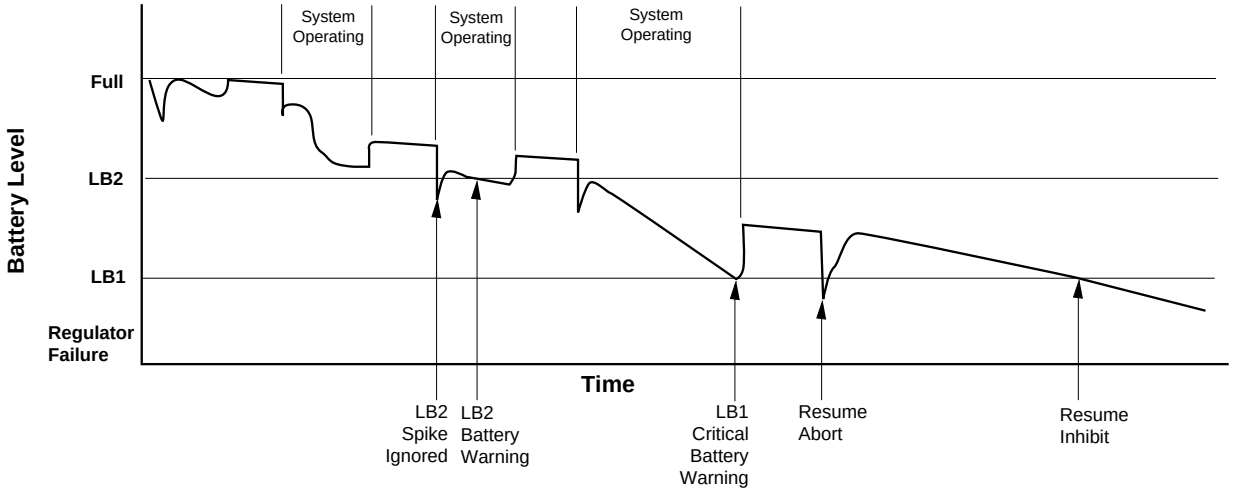
POWER MANAGEMENT UNIT (PMU) STATE DIAGRAM

Appendix C
Advanced Battery Monitoring

Advanced Battery Monitoring

Advanced Battery Monitoring provides improved reliability of user data. Figure C-1 shows how a battery charge level typically drops over time and crosses the associated battery warning level points (LB1 and LB2). The LB2 spike is ignored because during SUSPEND, the VG330 disables LB2 monitoring until after the inrush current that occurs during a transition to the ON state.

Figure C-1
Battery Life Curve



The VG330 is designed to address OEM concerns for reliability of battery operation. All aspects of battery operations can be managed by the VG330. The VG330 can monitor battery and power supply operation with several levels of low battery monitoring. In a system that implements two low battery levels (LB1 and LB2), the LB2 battery level is the critical battery warning to protect the user's data. LB1 then becomes a warning level only.

The LB1 warning level is usually set so that the user has a certain amount of time left to complete his tasks before shutting down his system. The LB2 warning level is usually set so that the system is suspended with enough power to keep the system data alive in memory until the batteries can be charged or replaced in typical replacement procedure.

Resume Abort can save data by resuspending quickly in response to batteries near exhaustion whose voltage level appears good until load is applied. As the software has not begun to operate yet, a critical battery event during this time can only be handled by the hardware itself. In addition, a hardware

timer is used to assure that system power good handshake signal is received within one second after resume starts. In this case, the user must immediately change the batteries because batteries near exhaustion will not keep the system powered very long even at the low power drawn in the SUSPEND state.

Resume Lockout can save data by refusing to start the resume process when the batteries are at low battery level. This prevents loss of remaining battery power caused by attempts to resume.

Fast Suspend takes place in a few milliseconds to save the contents of RAM that relies on the backup battery when the main battery is removed by the user during operation. Fast Suspend is a crucial feature if handheld device battery replacement is to be as simple as replacing a cellular phone battery.

The SmartBattery interface standard can be accommodated using the VG330 GPIO pins, if desired.