VG-CD1400

Data Book

FEATURES

Asynchronous Features

- **Software-programmable serial data rates up to 230.4 kbps, full-duplex**[1]
- **Twelve bytes of FIFO for each transmitter and each receiver, with programmable threshold for receive-FIFO-interrupt generation**
- **Improved interrupt schemes: Good Data™ interrupts eliminate the need for character status check**
- **Independent bit rate selection for transmit and receive on each channel**
- **User-programmable and automatic flow control modes for the serial channels:**
  - — In-band (software) flow control via single character (XON/XOFF)
  - — Out-of-band (hardware) flow control via RTS/CTS and DTR/DSR
- **Special character recognition and generation**

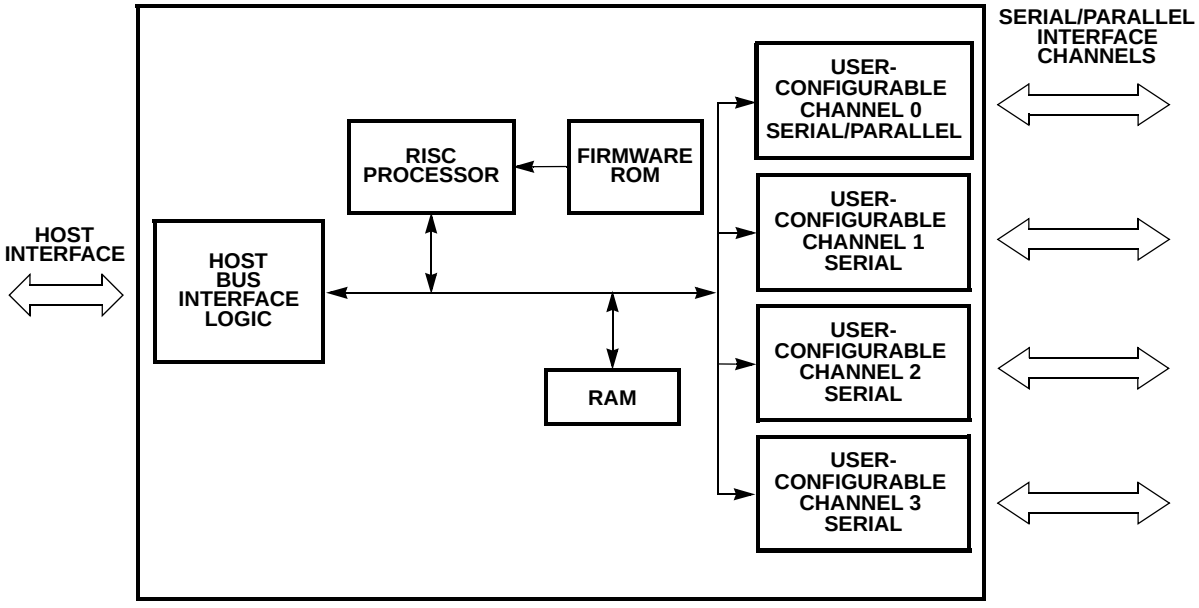
(cont.)

Four-Channel Serial/Parallel Communications Engine with UNIX® Character Processing

OVERVIEW

The VG-CD1400[2] is a flexible asynchronous receiver/transmitter with four full-duplex serial channels, or three full-duplex serial channels and one high-speed bidirectional parallel channel. With optional special character processing capabilities, it is especially well-suited for UNIX applications. The VG-CD1400 is fabricated in an advanced-CMOS process and operates on a system clock of up to 60 MHz. Packaged in a 100-pin PQFP[3], its high throughput, low-power consumption and high level of integration permit system designs with minimum part-count, maximum performance and maximum reliability.

Functional Block Diagram



FEATURES *(cont.)*

- **Special character processing, particularly useful for UNIX-line-driver applications, optionally handled automatically by the VG-CD1400**
  - Automatic expansion of NL to CR-NL
  - Supports LNEXT and ISTRIP
  - Ignore Break
  - UNIX parity handling options:
    - Character removed from stream
    - Passed as Good Data™
    - Replaced with null (00 hex)
    - Preceded with FF-00 hex
    - Passed as is with exception flagged
- **Line break detection (start and end) and generation, with programmable choice of response and data pattern to the host**
- **Insertion of transmit delays in data stream**
- **One timer per channel for receive data time-out interrupt**
- **Six modem control signals-per-channel (DTRDSR, RTS, CTS, CD, RI); CD and RI Signals not available if using the parallel channel**
- **Local and Remote Maintenance Loopback Modes**
- **Five to eight data bits per character plus optional parity**
- **Odd, even, no, or forced parity**
- **1, 1.5, or 2 Stop bits**

Parallel Features

- **Parallel data rates up to 105-Kbytes/sec. receive and 32-Kbytes/sec. transmit**
- **Thirty-byte FIFO**
- **Programmable strobe pulse widths**
- **Automatic generation and recognition of handshake control signals (STROBE, ACK, BUSY)**
- **Compatible with Centronics®-interface specifications**
- **New bits provided to increase parallel signal width**

CONFIGURATION EXAMPLES

Figures 1-1 through 1-3 on pages 8–9 are functional block diagrams of three possible configurations that can be implemented with the VG-CD1400. The first is a typical workstation with printer, mouse, keyboard and modem ports, a mode that includes a single parallel port and three serial channels with modem control; Figure 1-2 illustrates one channel with complete bidirectional modem control and three channels with partial modem control; Figure 1-3 shows a quad serial mode of four channels with complete modem control. All modes of operation are software-programmable through Control registers within the VG-CD1400.

FOOTNOTES:

1) A minimum clock frequency of 60 MHz is required to run all four serial channels at a 230.4-kbps data rate. Refer to the AC characteristics (Section 6 on page 135) for complete information on device timing.
2) This document applies to the VG-CD1400 Revision J or later device.
3) The VG-CD1400 is only offered in a 100-pin PQFP package.

DESIGN CONSIDERATIONS

The VG-CD1400 Revision J is a higher speed version of the VG-CD1400 Revision G. The VG-CD1400 Revision J is *only* available in a 100-pin PQFP package.

It is recommended that the VG-CD1400 Revision J be used for any new designs. Please note that to achieve the high data rates, a 60-MHz clock is required. Please refer to the pin differences between the VG-CD1400 Revision G and J.

Pin Differences

Feature	VG-CD1400 Revision J	VG-CD1400 Revision G
Package	100-pin PQFP	100-pin PQFP 68-pin PLCC
System clock	60 MHz	25 MHz
Maximum bit rates	230.4 kbps	115.2 kbps
Ground pins	13	4
V_{CC} pins	8	3
No-connect pins	15	29

NOTES:

1) Some of the no-connect pins on the VG-CD1400 Revision G (100-pin PQFP) were converted to additional V_{CC} and ground pins on the VG-CD1400 Revision J (please refer to the pin list on page 12 for details).
2) The VG-CD1400 Revision G part does not work in a Revision J layout. The Revision G no-connect pins must be left as true no-connect pins and cannot be connected to V_{CC} or Ground.
3) To achieve the high data rates, a 60-MHz system clock is required. However, it is not possible to achieve some low bit rates based on a 60-MHz clock (a lower system clock is required). Refer to Section 4.5 on page 78 for bit-rate programming constraints.

   Higher clock rates produce shorter PSTROBE* signal pulse widths, so when Channel 0 is programmed as a parallel port, similar limitations must also be considered (see Section 3.10 on page 58 for PSTROBE* pulse-width programming constraints).